ISO308x Isolated 5-V Full- and Half-Duplex RS-485 Transceivers

1 Features

- Meets or Exceeds TIA/EIA RS-485 Requirements
- Signaling Rates up to 20 Mbps
- 1/8 Unit Load – Up to 256 Nodes on a Bus
- Thermal Shutdown Protection
- Low Bus Capacitance – 16 pF (Typical)
- 50 kV/μs Typical Transient Immunity
- Fail-safe Receiver for Bus Open, Short, Idle
- 3.3-V Inputs are 5-V Tolerant
- Bus-Pin ESD Protection
  - 12 kV HBM Between Bus Pins and GND2
  - 6 kV HBM Between Bus Pins and GND1
- Safety and Regulatory Approvals
  - 4000-V_{PK} Basic Insulation, 560 V_{PK} V_{IORM} per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 and DIN EN 61010-1
  - 2500 V_{RMS} Isolation per UL 1577
  - 4000 V_{PK} Isolation per CSA Component Acceptance Notice 5A and IEC 60950-1

2 Applications

- Security Systems
- Chemical Production
- Factory Automation
- Motor and Motion Control
- HVAC and Building Automation Networks
- Networked Security Stations

3 Description

The ISO3080 and ISO3086 devices are isolated full-duplex differential line drivers and receivers while the ISO3082 and ISO3088 devices are isolated half-duplex differential line transceivers for TIA/EIA 485/422 applications.

These devices are ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 2500 Vrms of isolation for 60s per UL 1577 between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or nearby sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

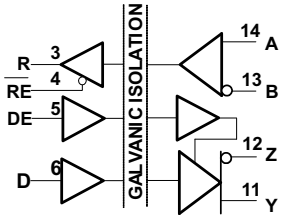
The ISO3080, ISO3082, ISO3086, and ISO3088 are qualified for use from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO3080	SOIC (16)	10.30 mm × 7.50 mm
ISO3082		
ISO3086		
ISO3088		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ISO3080, IOS3086 Function Diagram



ISO3082, IOS3088 Function Diagram

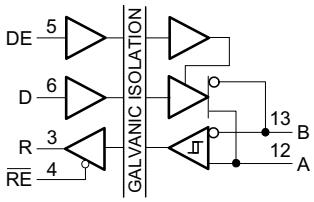


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (July 2015) to Revision H — **Page**

- Changed the CDM value in *ESD Ratings* From: ±200 To: ±1000 ... 5
- Changed the MON value of L(IO1) in Table 1 From: 8.34 To: 8 mm ... 15
- Changed the MON value of L(IO2) in Table 1 From: 8.1 To: 8 mm ... 15
- Moved the last list item " Routing the high-speed traces..." to the second list items in *Layout Guidelines* section ... 21

Changes from Revision F (May 2015) to Revision G — **Page**

- Deleted "Rated mains voltage ≤ 400 V_{RMS}" from Table 3 ... 15
- Changed "Maximum case temperature" To: "Maximum safety temperature" in Table 5 ... 16
- Changed the *Layout Guidelines* section ... 21

Changes from Revision E (September 2011) to Revision F — **Page**

- Added *ESD Rating* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging*, and *Orderable* Information section ... 1
- Changed *Features* list item From: IEC 60747-5-2 (VDE 0884, Rev. 2) To: DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ... 1
- VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ... 1
- Changed Table 3. Basic isolation group SPECIFICATION entry From: IIIa To: II ... 15

Changes from Revision D (January 2011) to Revision E **Page**

- Changed *Features* list item From: 16 kV HBM To: 12 kV HBM ... 1
- Changed ESD HBM spec value from ±16 to ±12 in *ESD Ratings* ... 5

Changes from Revision C (October 2009) to Revision D **Page**

- Added T_{STG} row to the *Absolute Maximum Ratings*(1) ... 5
- Added "Dynamic" conditions to *Recommended Operating Conditions* V_{ID} spec with reference to Figure 9 ... 5
- Changed for 3 V to 3.3 V in note 1 of the *Recommended Operating Conditions* table ... 5
- Deleted $V_I = V_{CCI}$ or 0 V from CMTI spec. Conditions statement. Added "Figure 13" in *Electrical Characteristics: Driver* ... 6
- Changed top row, UNIT column, split into 2 rows, top row µs and second row ns in *Switching Characteristics: Driver* ... 7
- Added Figure 9 ... 8
- Added note to bottom of first page of the *Parameter Measurement Information* ... 10
- Changed File Number from '1698195' to '220991 in Table 4 ... 15
- Changed θ_{JA} from 212 ° C/W to 168 ° C/W in conditions statement for I_S spec.; and MAX current from 210 mA to 157 mA in Table 5 ... 16
- Changed graph for " DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5-2 " , Figure 25 ... 16
- Added Footnotes to the Table 6 and Table 7 ... 17

Changes from Revision B (December 2008) to Revision C **Page**

- Changed *Recommended Operating Conditions* table note From: For 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6V. To: For 3-V operation, V_{CC1} is specified from 3.15 V to 3.6V. ... 5

Changes from Revision A (June 2008) to Revision B **Page**

- Changed *Features* bullet From: 4000-V_{PEAK} Isolation, To: 4000-V_{PEAK} Isolation,, 560-V_{PEAK} V_{IORM} ... 1
- Added the CSA column to Table 4 ... 15

Changes from Original (May 2008) to Revision A **Page**

- Deleted the CSA column from Table 4. ... 15
- Changed the file number in the VDE column in Table 4 From: 40014131 To: 40016131 ... 15

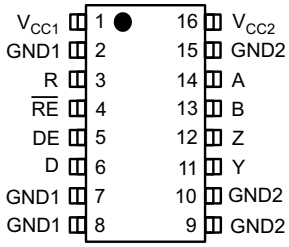
5 Device Comparison Table

DEVICE	RATED ISOLATION(1)	TYPE	DATA RATE
ISO3080	4000 V_{PK} / 2500 V_{RMS}	Full-duplex	200 kbps
ISO3086	4000 V_{PK} / 2500 V_{RMS}	Full-duplex	20 Mbps
ISO3082	4000 V_{PK} / 2500 V_{RMS}	Half-duplex	200 kbps
ISO3088	4000 V_{PK} / 2500 V_{RMS}	Half-duplex	20 Mbps

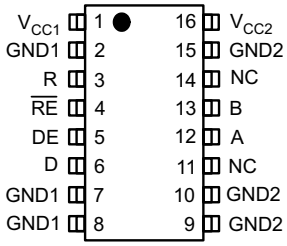
(1) See the *Table 4* table for detailed isolation ratings.

6 Pin Configuration and Functions

DW Package ISO3080, ISO3086
16-Pin SOIC
Top View



DW Package ISO3082, ISO3088
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO3080, ISO3086	ISO3082, ISO3088		
A	14	--	I	Receiver noninverting input on the bus-side
	--	12	I/O	Transceiver noninverting Input or Output (I/O) on the bus-side
B	13	--	I	Receiver inverting Input on the bus-side
	--	13	I/O	Transceiver inverting Input or Output (I/O) on the bus-side
D	6	6	I	Driver Input
DE	5	5	I	Enables (when High) or Disables (when Low or Open) Driver output of ISO308x
GND1	2, 7, 8	2, 7, 8	–	Ground connection for V_{CC1}
GND2	9, 10, 15	9, 10, 15	–	Ground connection for V_{CC2}
NC	--	11, 14	–	No Connect
R	3	3	O	Receiver Output
$\overline{RE}$	4	4	I	Disables (when High or Open) or Enables (when Low) Receiver Output of ISO308x
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	–	Power supply, V_{CC2}
Y	11	--	O	Driver noninverting output
Z	12	--	O	Driver inverting output

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC}	Input supply voltage, (2) V_{CC1}, V_{CC2}	–0.3	6	V
V_O	Voltage at any bus I/O terminal	–9	14	V
V_{IT}	Voltage input, transient pulse, A, B, Y, and Z (through 100Ω, see Figure 20)	–50	50	V
V_I	Voltage input at any D, DE or $\overline{RE}$ terminal	–0.5	7	V
I_O	Receiver output current		±10	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	Bus pins and GND1	±6000	V
			Bus pins and GND2	±12000	
			All pins	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	All pins	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC1}	Logic-side supply voltage (1)		3.15		5.5	V
V_{CC2}	Bus-side supply voltage(1)		4.5	5	5.5	V
V_{OC}	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		VCC	V
V_{IL}	Low-level input voltage		0		0.8	
V_{ID}	Differential input voltage	A with respect to B	–12		12	V
		Dynamic (ISO3086)	see Figure 9			
R_L	Differential input resistance		54	60		Ω
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
T_A	Ambient temperature		–40		85	°C

(1) For 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For 3.3-V operation, V_{CC1} is specified from 3.15 V to 3.6 V.

7.4 Thermal Information

THERMAL METRIC(1)			ISO308x DW 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K thermal resistance(2)	168	°C/W
		High-K thermal resistance	79.6	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		39.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		44.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter		11.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter		44.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

7.5 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage magnitude	I_O = 0 mA, no load			3	4.3	V_{CC}	V
		R_L = 54 Ω, See Figure 10			1.5	2.3		
		R_L = 100 Ω (RS-422), See Figure 10			2	2.3		
		V_{test} from –7 V to +12 V, See Figure 11			1.5			
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of the differential output voltage	See Figure 10 and Figure 11			–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 12			1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.1		0.1	
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	See Figure 12				0.5		V
I_I	Input current	D, DE, V_I at 0 V or V_{CC1}			–10		10	µA
I_{OZ}	High-impedance state output current	ISO3082 ISO3088	See receiver input current					
		ISO3080 ISO3086	V_Y or V_Z = 12 V, V_{CC} = 0 V or 5 V, DE = 0 V	Other input at 0 V			1	µA
			V_Y or V_Z = –7 V. V_{CC} = 0 V or 5 V, DE = 0 V		–1			
I_{OS}	Short-circuit output current	V_A or V_B at –7 V		Other input at 0 V	–200		200	mA
		V_A or V_B at 12 V						
CMTI	Common-mode transient immunity	See Figure 21 and Figure 22			25	50		kV/µs

7.6 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going input threshold voltage	I_O = –8 mA			–85	–10	mV
$V_{IT(–)}$	Negative-going input threshold voltage	I_O = 8 mA		–200	–115		mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)				30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_O = –8 mA, See Figure 16	3.3-V V_{CC1}	V_{CC1}-0.4	3.1		V
			5-V V_{CC1}	4	4.8		
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_O = 8 mA, See Figure 16	3.3-V V_{CC1}		0.15	0.4	V
			5-V V_{CC1}		0.15	0.4	
$I_{O(Z)}$	High-impedance state output current	V_I = –7 to 12 V, Other input = 0 V		–1		1	µA
I_I	Bus input current	V_A or V_B = 12 V	Other input at 0 V		0.04	0.1	mA
		V_A or V_B = 12 V, V_{CC} = 0			0.06	0.13	
		V_A or V_B = –7 V		–0.1	–0.04		
		V_A or V_B = –7 V, V_{CC} = 0		–0.05	–0.03		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V		–10		10	µA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V		–10		10	µA
R_{ID}	Differential input resistance	A, B		48			kΩ
C_D	Differential input capacitance	Test input signal is a 1.5 MHz sine wave with 1Vpp amplitude. C_D is measured across A and B.			7		pF

7.7 Supply Current

over recommended operating condition (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	Logic-side supply current	$\overline{RE}$ at 0 V or V_{CC}, DE at 0 V or V_{CC1}	3.3-V V_{CC1}			8	mA
		$\overline{RE}$ at 0 V or V_{CC}, DE at 0 V or V_{CC1}	5-V V_{CC1}			10	
I_{CC2}	Bus-side supply current	$\overline{RE}$ at 0 V or V_{CC}, DE at 0 V, No load				15	mA

7.8 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO3080/82		See Figure 13		0.7	1.3	µs
		ISO3086/88				25	45	ns
PWD(1)	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	ISO3080/82				20	200	ns
		ISO3086/88				3	7.5	
t_r, t_f	Differential output signal rise and fall time	ISO3080/82			0.5	0.9	1.5	µs
		ISO3086/88				7	15	ns
t_{PZH}, t_{PZL}	Propagation delay, high-impedance-to-high-level output Propagation delay, high-impedance-to-low-level output	ISO3080/82	50% Vo	See Figure 14 and Figure 15, DE at 0 V		2.5	7	µs
			90% Vo			1.8		
		ISO3086/88				25	55	ns
t_{PHZ}, t_{PLZ}	Propagation delay, high-level-to-high-impedance output Propagation delay, low-level to high-impedance output	ISO3080/82				95	225	ns
		ISO3086/88				25	55	

(1) Also known as pulse skew

7.9 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 17		90	125	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			4	12	
t_r, t_f	Output signal rise and fall time			1		ns
t_{PHZ}, t_{PZH}	Propagation delay, high-level-to-high-impedance output Propagation delay, high-impedance-to-high-level output	See Figure 18, DE at 0 V			22	ns
t_{PZL}, t_{PLZ}	Propagation delay, high-impedance-to-low-level output Propagation delay, low-level-to-high-impedance output	See Figure 19, DE at 0 V			22	ns

(1) Also known as pulse skew.

7.10 Typical Characteristics

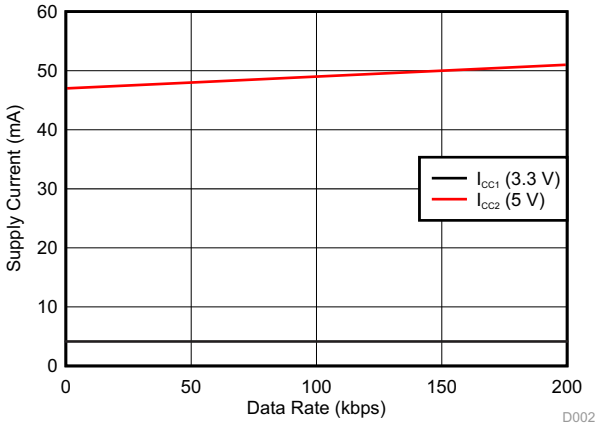


Figure 1. ISO3080 Supply Current vs Data Rate With Load

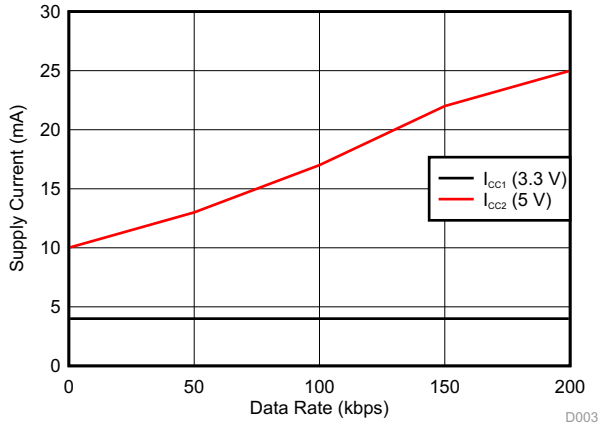


Figure 2. ISO3080 Supply Current vs Data Rate With No Load

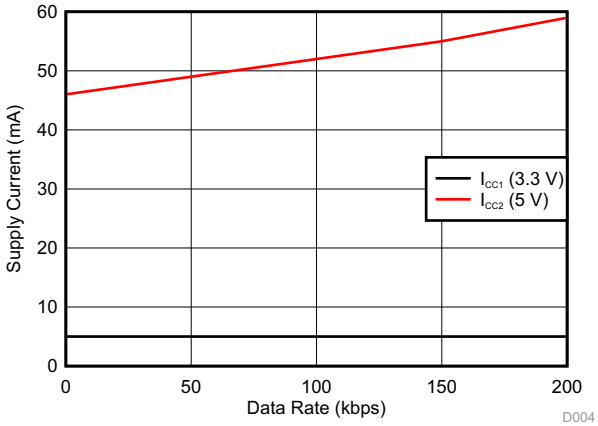


Figure 3. ISO3082 Supply Current vs Data Rate With Load

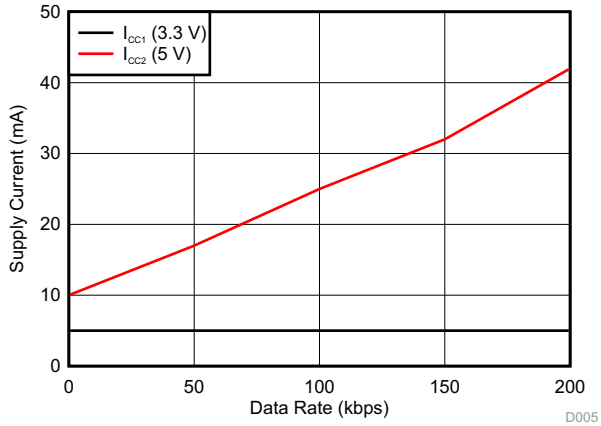


Figure 4. ISO3082 Supply Current vs Data Rate With No Load

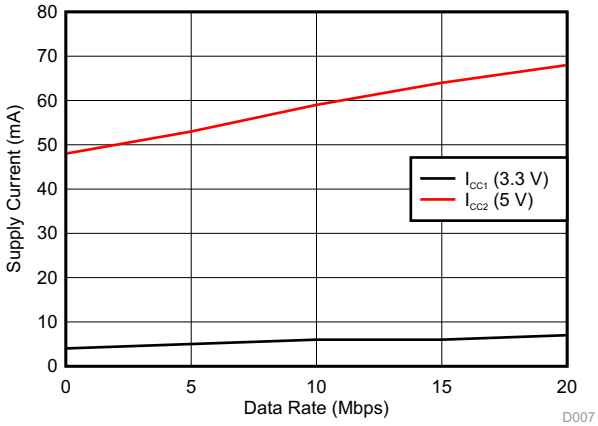


Figure 5. ISO3086 Supply Current vs Data Rate With Load

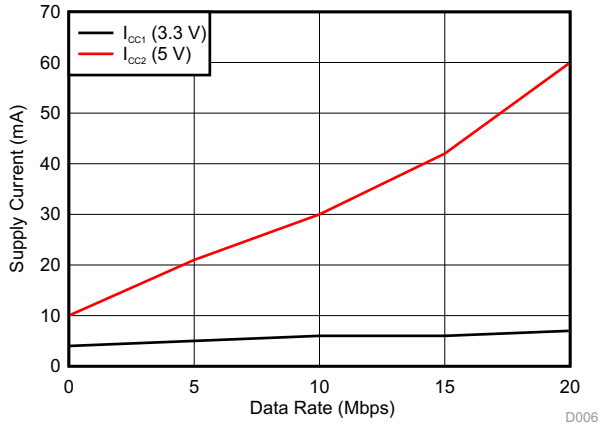


Figure 6. ISO3086 Supply Current vs Data Rate With No Load

Typical Characteristics (continued)

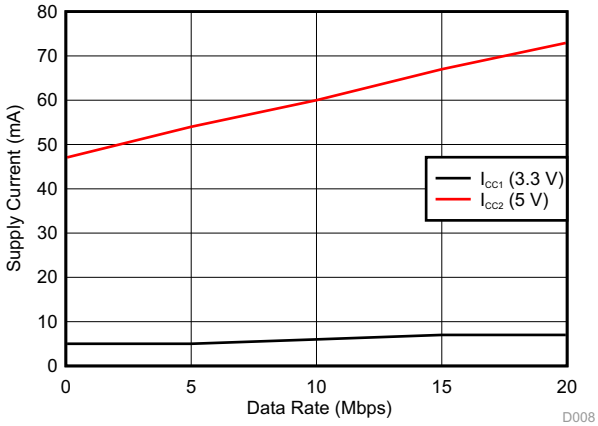


Figure 7. ISO3088 Supply Current vs Data Rate With Load

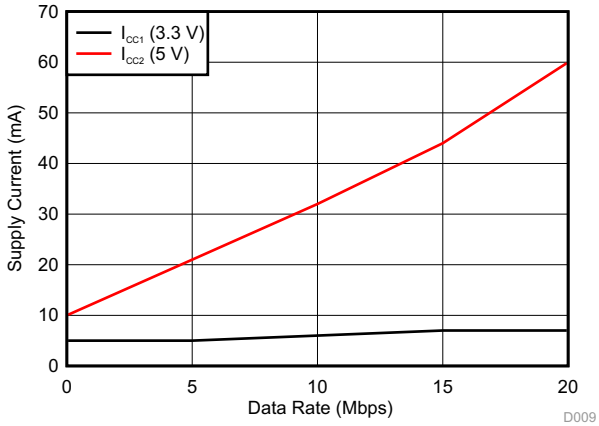


Figure 8. ISO3088 Supply Current vs Data Rate With No Load

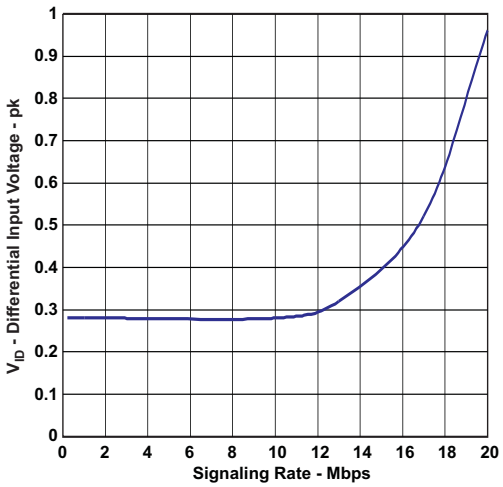


Figure 9. ISO3086 Recommended Minimum Differential Input Voltage vs Signaling Rate

8 Parameter Measurement Information

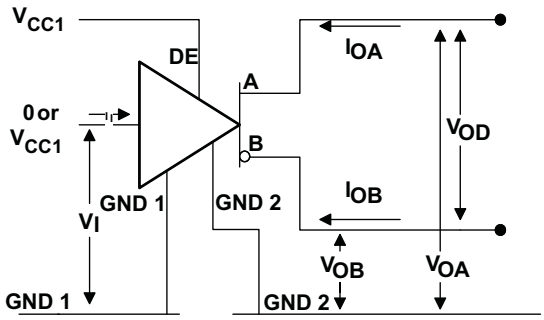


Figure 10. Driver V_{OD} Test and Current Definitions

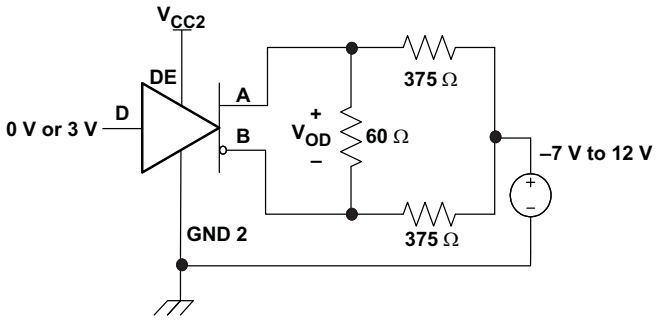


Figure 11. Driver V_{OD} With Common-Mode Loading Test Circuit

Note: Unless otherwise stated, test circuits are shown for half-duplex devices, ISO3082 & ISO3088. For full-duplex devices, driver output pins are Y and Z.

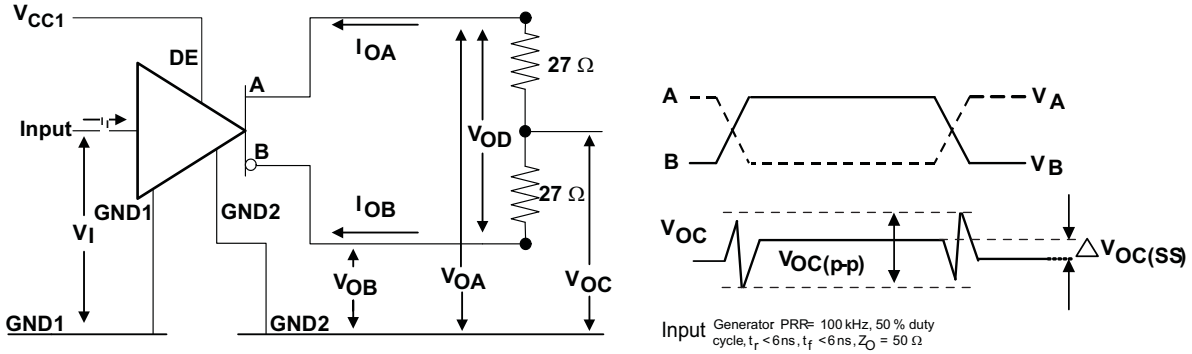


Figure 12. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage

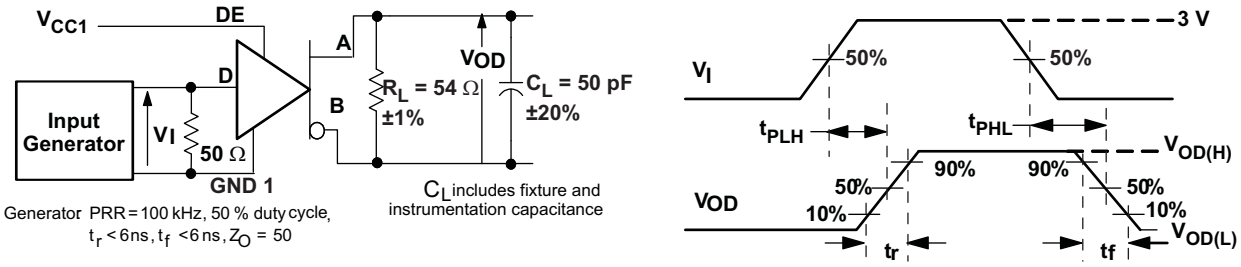


Figure 13. Driver Switching Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

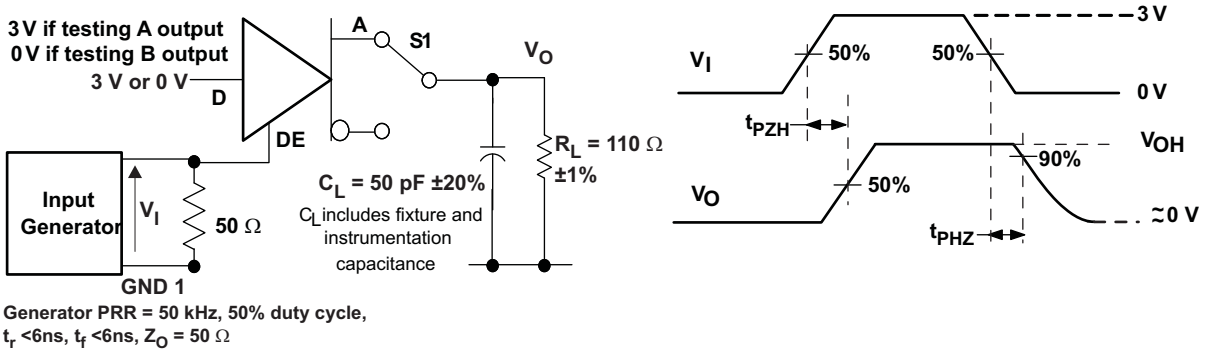


Figure 14. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

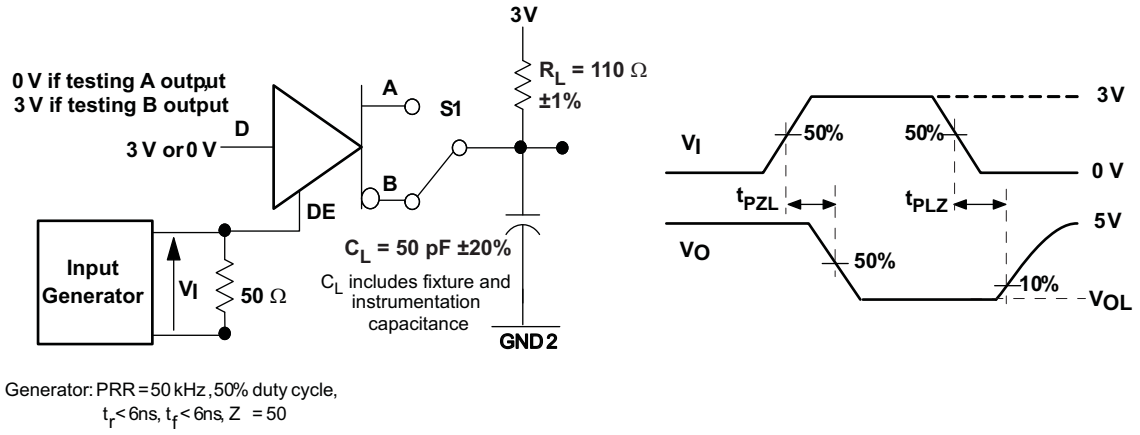


Figure 15. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

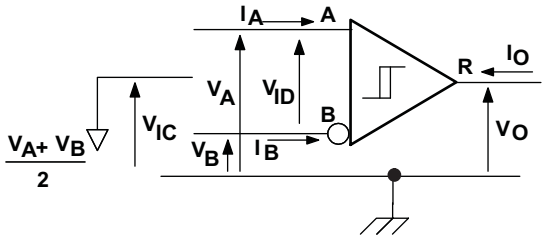


Figure 16. Receiver Voltage and Current Definitions

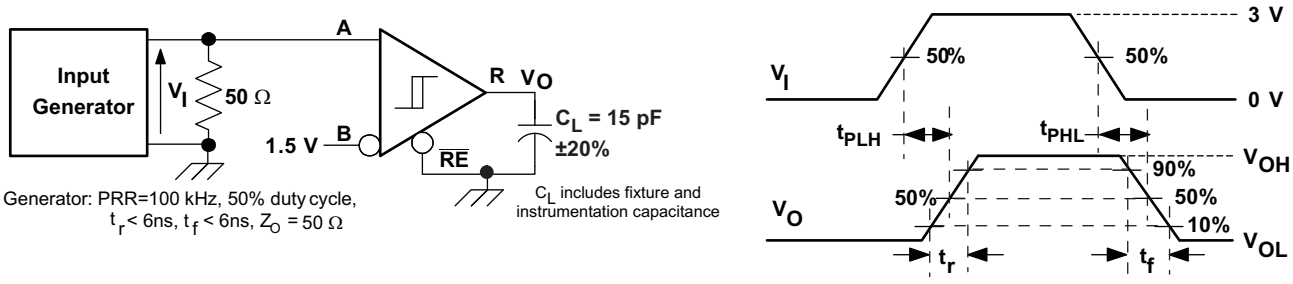


Figure 17. Receiver Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)

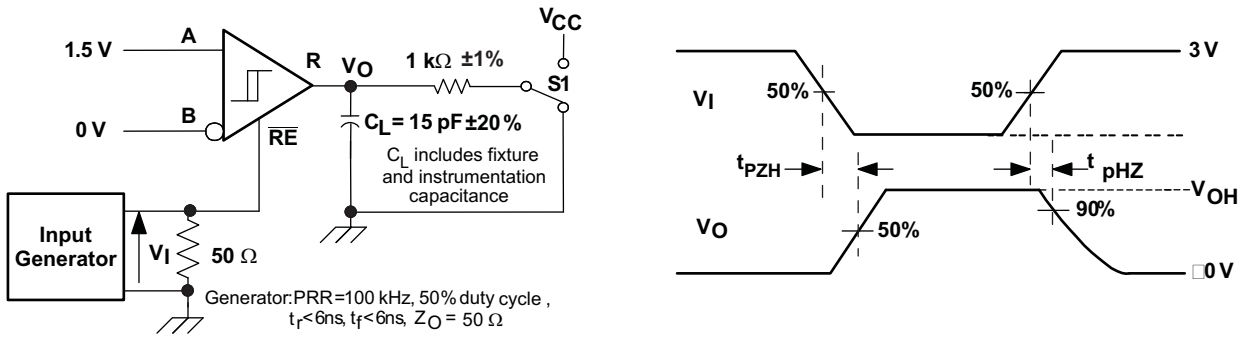


Figure 18. Receiver Enable Test Circuit and Waveforms, Data Output High

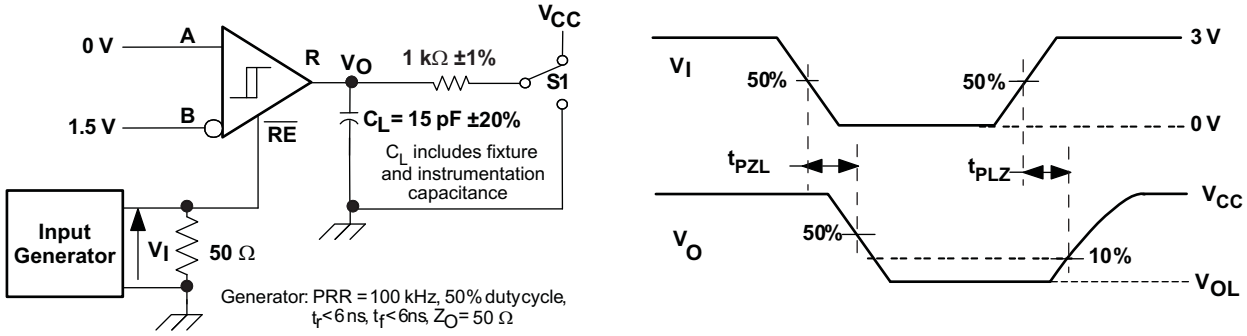
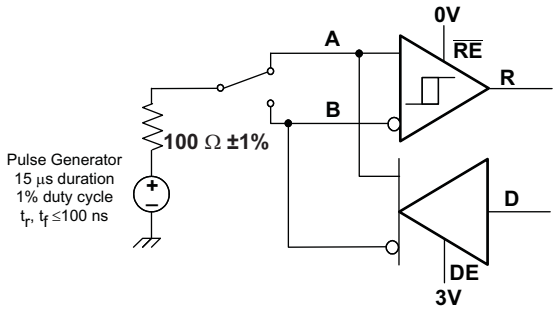


Figure 19. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only.
Data stability at the R output is not specified.

Figure 20. Transient Overvoltage Test Circuit

Parameter Measurement Information (continued)

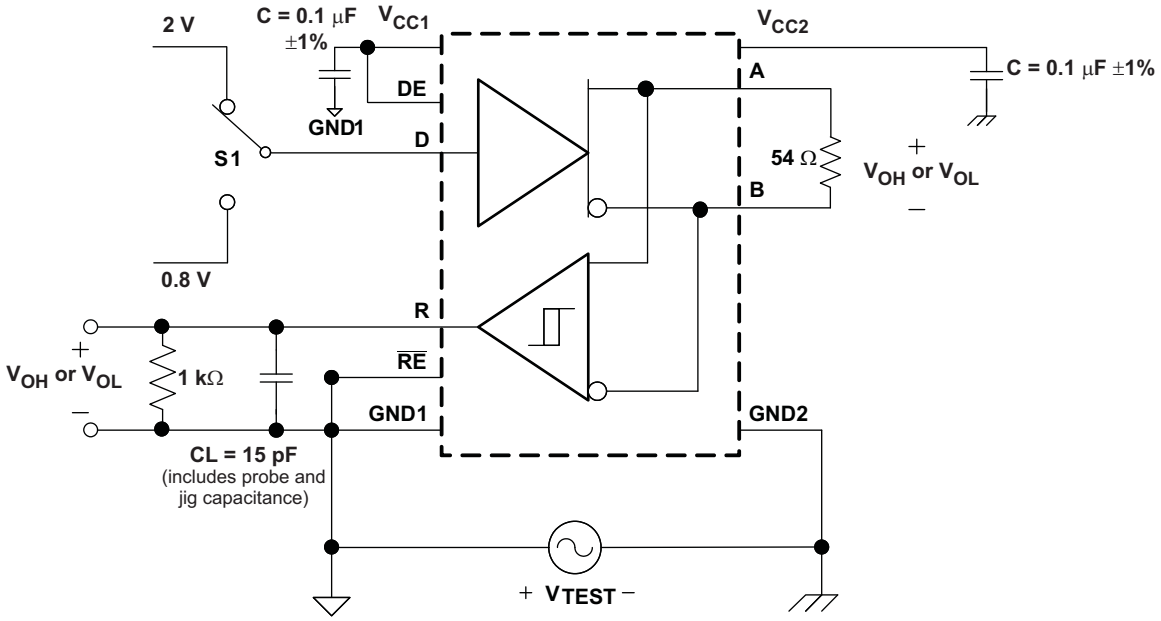


Figure 21. Half-Duplex Common-Mode Transient Immunity Test Circuit

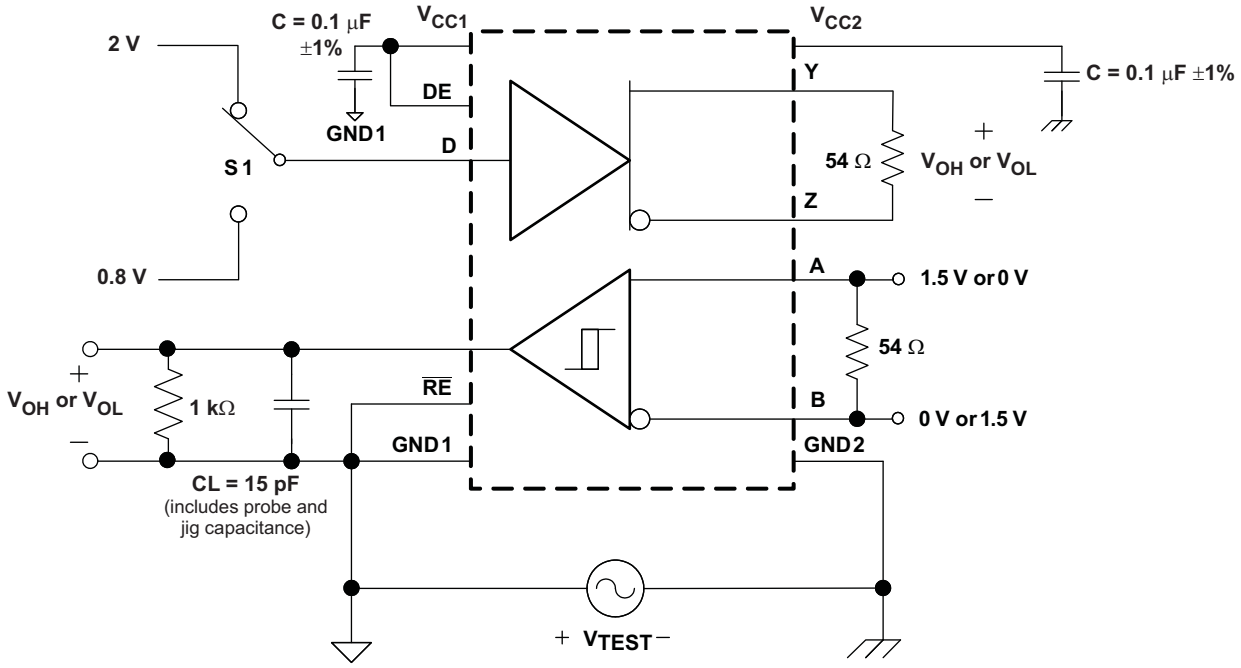


Figure 22. Full-Duplex Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ISO3080, and ISO3086 are isolated full-duplex differential line drivers and receivers while the ISO3082, and ISO3088 are isolated half-duplex differential line transceivers for TIA/EIA 485/422 applications. They are rated to provide galvanic isolation of up to 2500 V_{rms} for 60 sec as per the standard. They have active-high driver enables and active-low receiver enables to control the data flow. They are available in two speed grades suitable for data transmission up to 200 kbps and 20 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_{(Y)} – V_{(Z)}$ is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

When the receiver enable pin, RE, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When RE is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

9.2 Functional Block Diagrams

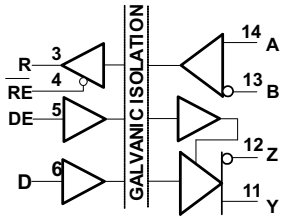


Figure 23. ISO3080, IOS3086 Functional Diagram

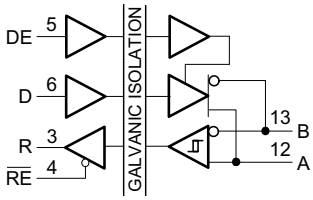


Figure 24. ISO3082, IOS3088 Functional Diagram

9.3 Feature Description

Table 1. Insulation and Safety-Related Package Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance) (1)	Shortest terminal-to-terminal distance through air	8			mm
L(I02)	Minimum external tracking (Creepage) (1)	Shortest terminal-to-terminal distance across the package surface	8			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
	Minimum internal gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, TA = 25°C, all pins on each side of the barrier tied together creating a 2-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance input to output	VI = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	VI = 0.4 sin (4E6πt)		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit-board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a PCB are used to help increase these specifications.

Table 2. DIN V VDE V 0884-10 Insulation Characteristics (1) over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOTM}	Transient overvoltage	Method a, t = 60 s, Qualification test	4000	V
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input to output test voltage	Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with t = 1 s, Partial discharge < 5 pC	1050	V
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 3. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-III

Table 4. Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Approved under CSA Component Acceptance Notice 5A and IEC 60950-1	Recognized under UL 1577 Component Recognition Program (1)
Basic insulation, 4000 V_{PK} Maximum transient overvoltage, 560 V_{PK} Maximum working voltage	4000 V_{PK} Isolation rating, 560 V_{PK} Basic working voltage per CSA 60950-1-07 and IEC 60950-1 (2nd Ed)	Single Protection, 2500 V_{RMS}
Certificate number: 40016131	Master contract number: 220991	File number: E181974

(1) Production tested ≥3000 V_{RMS} for 1 second in accordance with UL 1577.

9.3.1 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

Table 5. Safety Limiting

PARAMETER				MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 79.6°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			286	mA
T_S	Maximum safety temperature	DW-16				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in a High-Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

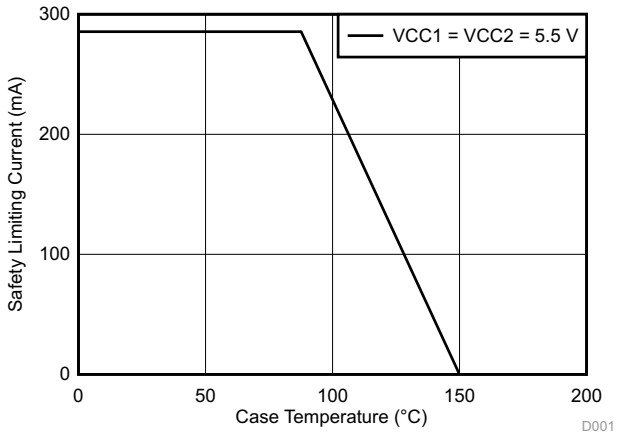


Figure 25. Thermal Derating Curve

9.4 Device Functional Modes

Table 6. Driver Function Table(1)

V_{CC1}	V_{CC2}	INPUT (D)	ENABLE INPUT (DE)	OUTPUTS(2)	
				Y / A	Z / B
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Hi-Z	Hi-Z
PU	PU	X	OPEN	Hi-Z	Hi-Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Hi-Z	Hi-Z
PU	PD	X	X	Hi-Z	Hi-Z
PD	PD	X	X	Hi-Z	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (off)
(2) Driver output pins are Y and Z for full-duplex devices and A and B for half-duplex devices.

Table 7. Receiver Function Table(1)

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
PU	PU	$-0.01\ V \le V_{ID}$	L	H
PU	PU	$-0.2\ V < V_{ID} < -0.01\ V$	L	?
PU	PU	$V_{ID} \le -0.2\ V$	L	L
PU	PU	X	H	Hi-Z
PU	PU	X	OPEN	Hi-Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Hi-Z
PU	PD	X	L	H

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (off), ? = Indeterminate

9.4.1 Device I/O Schematics

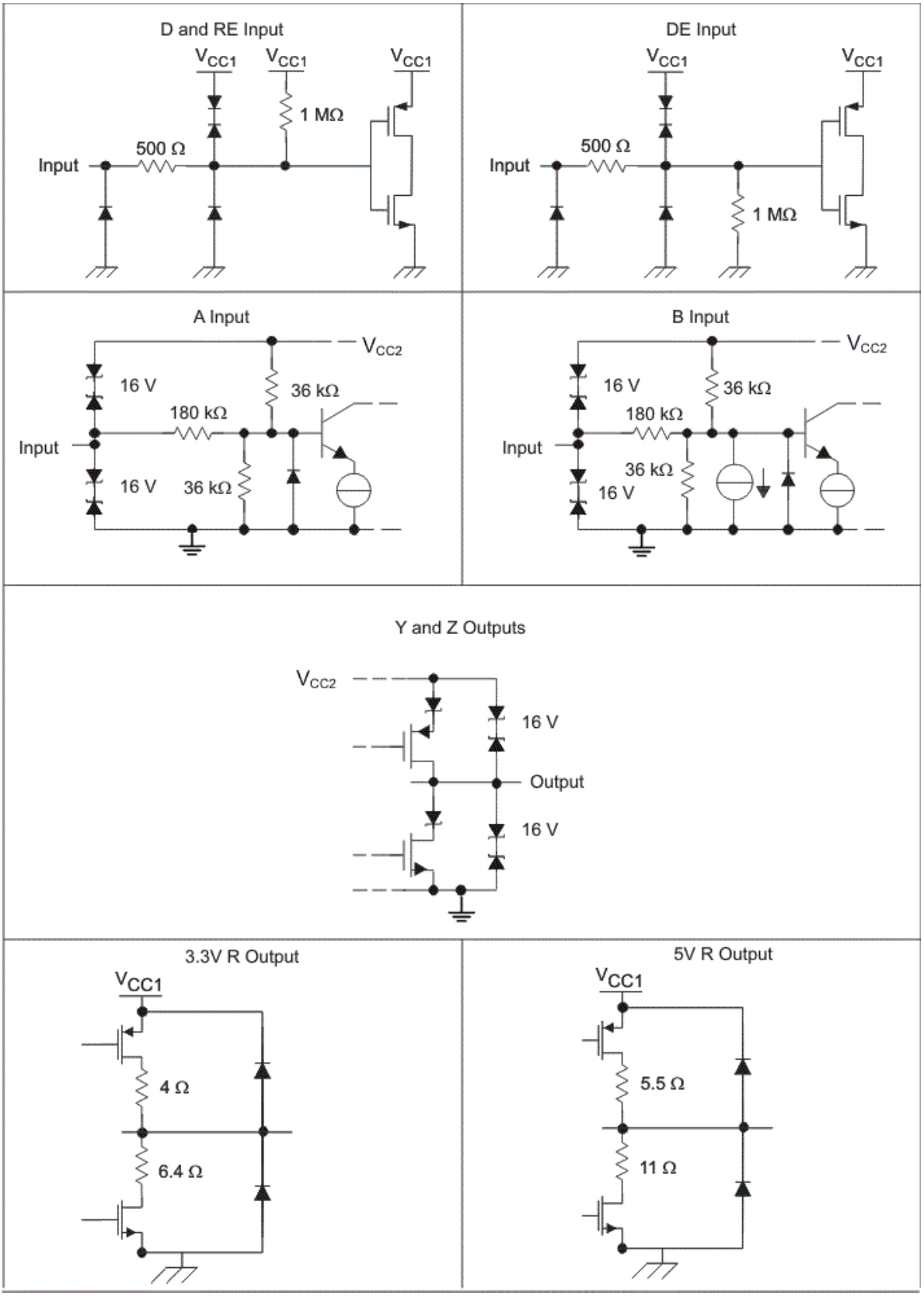


Figure 26. Device I/O Schematics

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO308x family consists of RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. For half-duplex transmission, only one pair is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

10.2 Typical Application

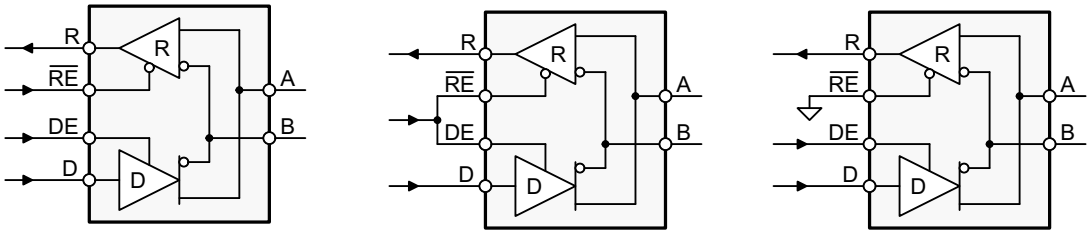


Figure 27. Half-Duplex Transceiver Configurations

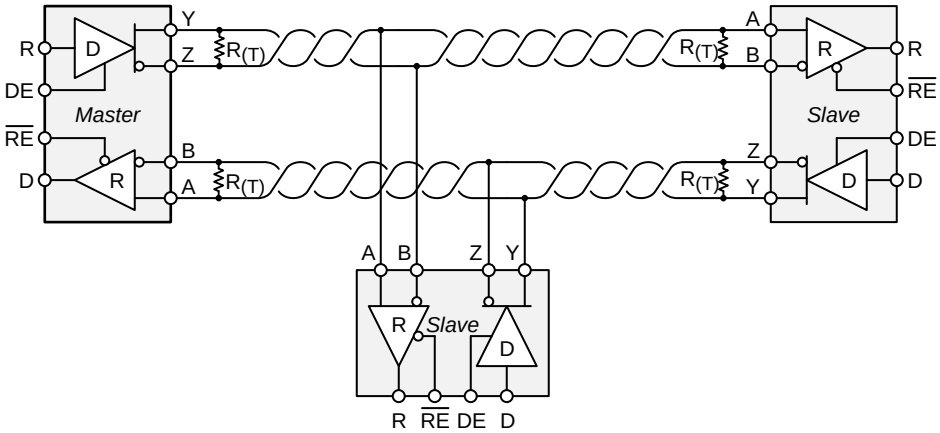


Figure 28. Typical RS-485 Network With Full-Duplex Transceivers

Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Table 8. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

10.2.2 Detailed Design Procedure

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver. The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (ULs), where 1 UL represents a load impedance of approximately 12 kΩ. Because the ISO308x family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

10.2.3 Application Curves

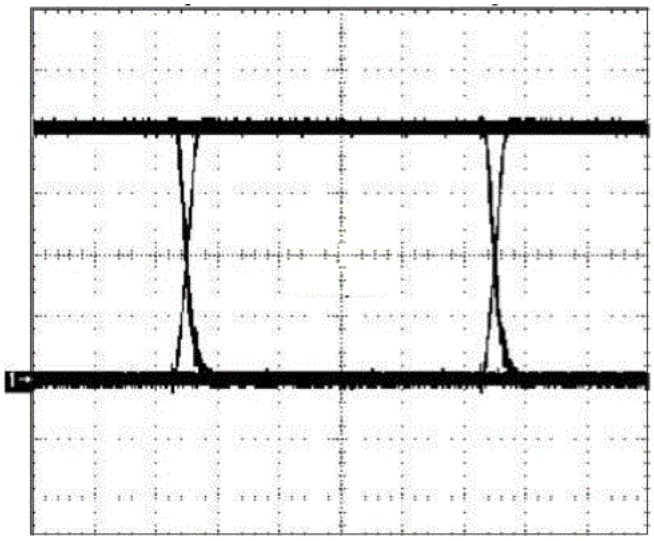


Figure 29. ISO308x Output

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

12 Layout

12.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 30).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1-µF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

Layout Guidelines (continued)

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

NOTE

Note: For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

12.2 Layout Example

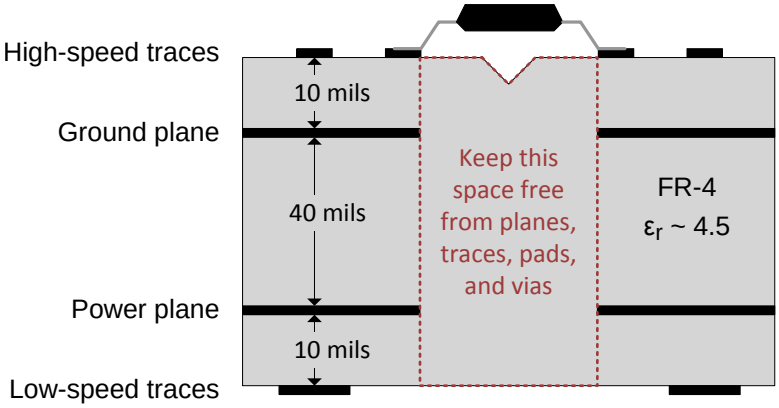


Figure 30. Recommended Layer Stack

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide*, SLLSEA0
- *Transformer Driver for Isolated Power Supplies*, SLLA284
- *Isolation Glossary*, SLLA353

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO3080	Click here	Click here	Click here	Click here	Click here
ISO3082	Click here	Click here	Click here	Click here	Click here
ISO3086	Click here	Click here	Click here	Click here	Click here
ISO3088	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

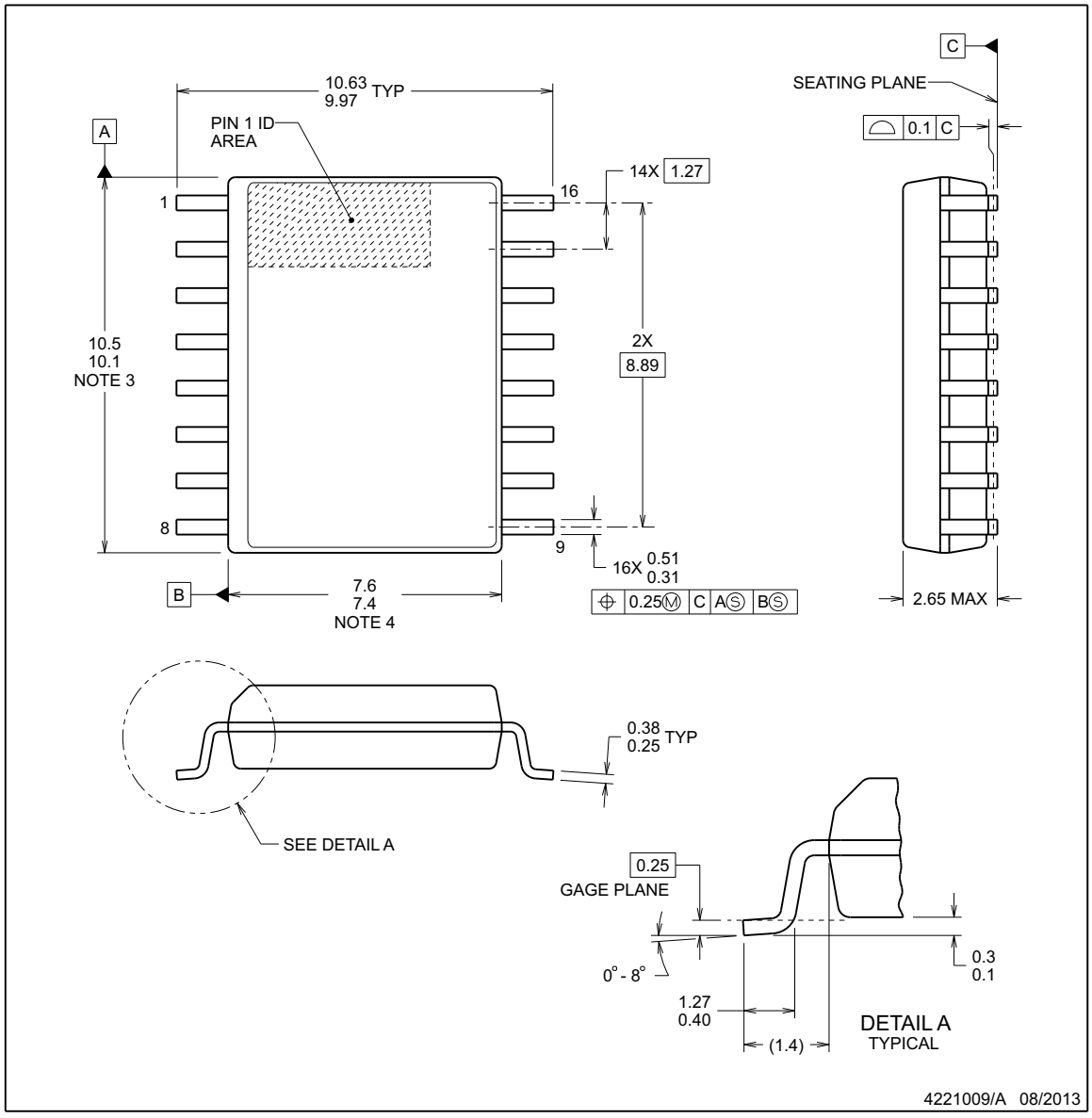
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

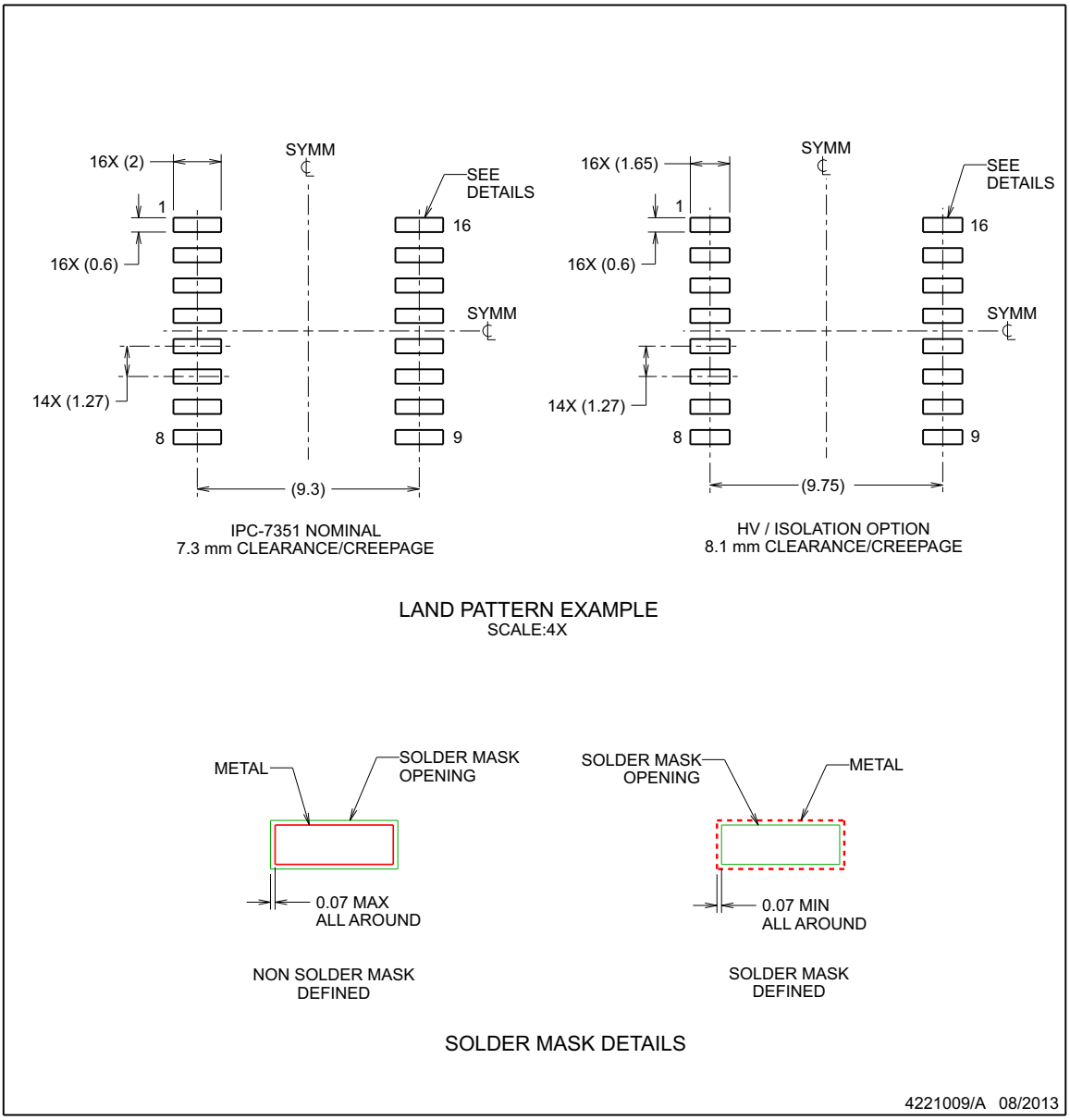
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



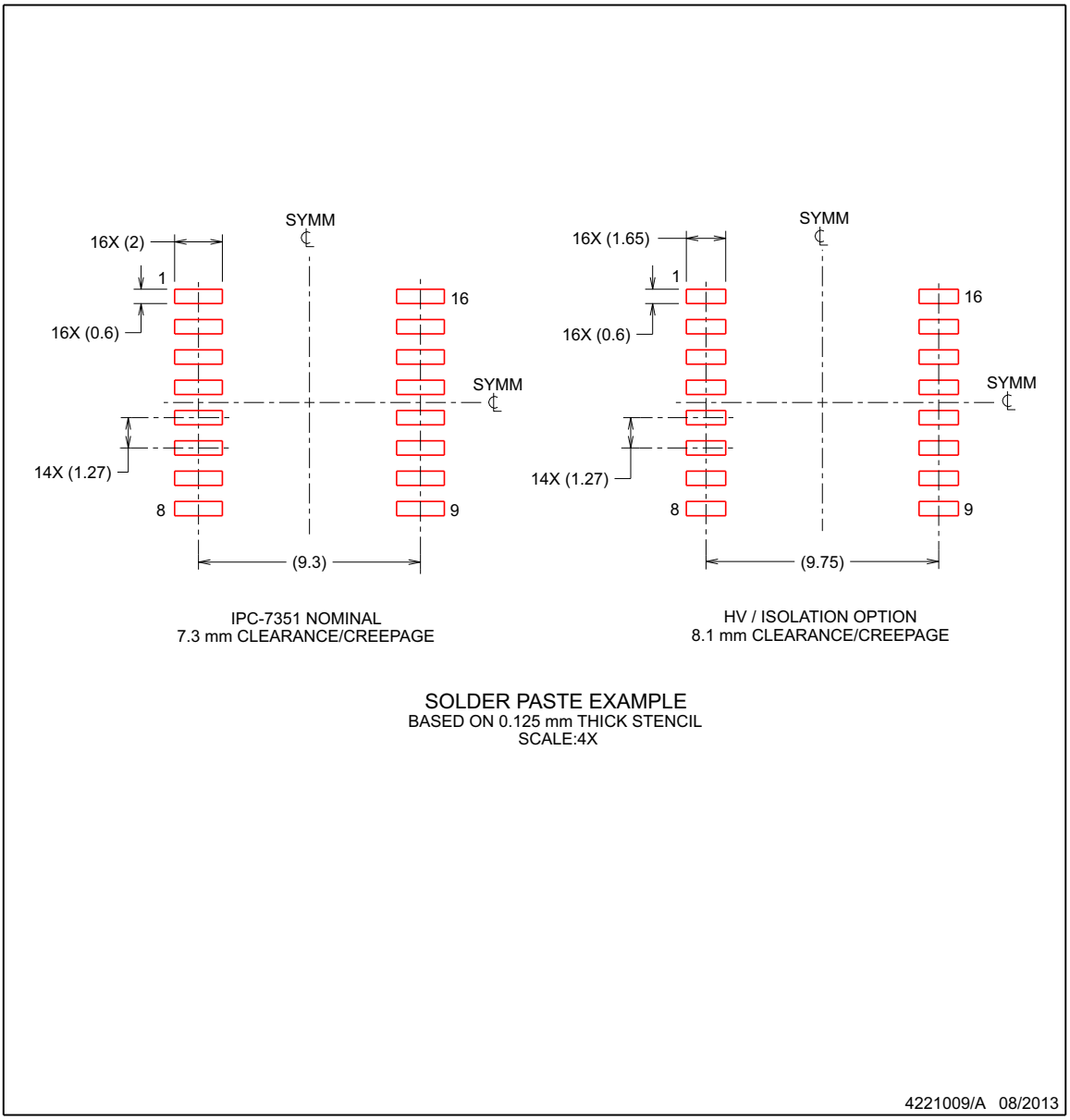
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B — SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO3080DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3080	Samples
ISO3080DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3080	Samples
ISO3080DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3080	Samples
ISO3080DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3080	Samples
ISO3082DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3082	Samples
ISO3082DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3082	Samples
ISO3082DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3082	Samples
ISO3082DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3082	Samples
ISO3086DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3086	Samples
ISO3086DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3086	Samples
ISO3086DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3086	Samples
ISO3088DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3088	Samples
ISO3088DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3088	Samples
ISO3088DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3088	Samples
ISO3088DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO3088	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

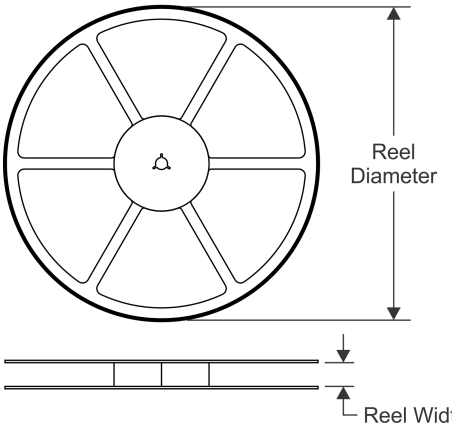
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

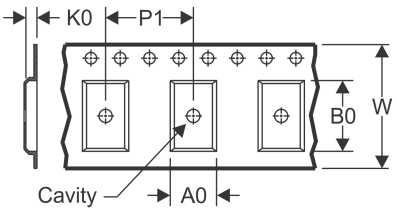
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

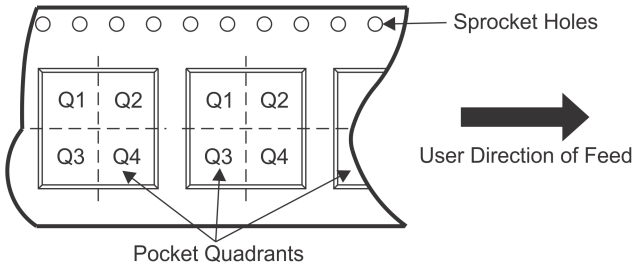


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

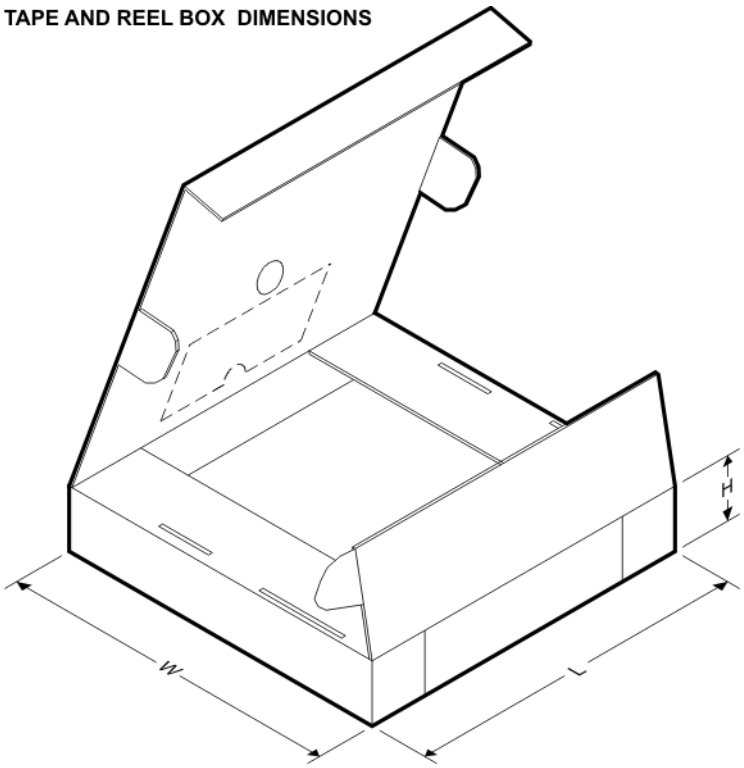
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO3080DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO3082DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO3086DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO3088DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO3080DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO3082DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO3086DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO3088DWR	SOIC	DW	16	2000	367.0	367.0	38.0

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