CD74HC390, CD74HCT390

High Speed CMOS Logic
Dual Decade Ripple Counter

September 1997

Features

- **Two BCD Decade or Bi-Quinary Counters**

- **One Package Can Be Configured to Divide-by-2, 4, 5,10, 20, 25, 50 or 100**

- **Two Master Reset Inputs to Clear Each Decade Counter Individually**

- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**

- **Wide Operating Temperature Range . . . -55°C to 125°C**

- **Balanced Propagation Delay and Transition Times**

- **Significant Power Reduction Compared to LSTTL Logic ICs**

- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The Harris CD74HC390 and CD574HCT390 dual 4-bit decade ripple counters are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These devices are divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs (n$\overline{CP0}$ and n$\overline{CP1}$) of each section allow ripple counter or frequency division applications of divide-by-2, 4. 5, 10, 20, 25, 50 or 100. Each section is triggered by the High-to-Low transition of the input pulses (n$\overline{CP0}$ and n$\overline{CP1}$).

For BCD decade operation, the nQ0 output is connected to the n$\overline{CP1}$ input of the divide-by-5 section. For bi-quinary decade operation, the nO3 output is connected to the n$\overline{CP0}$ input and nQ$_0$ becomes the decade output.

The master reset inputs (1MR and 2MR) are active-High asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A High level on the nMR input overrides the clock and sets the four outputs Low.

Pinout

CD74HC390, CD74HCT390
TOP VIEW

Pin			Pin
1$\overline{CP0}$	1	16	V_{CC}
1MR	2	15	2$\overline{CP0}$
1Q$_0$	3	14	2MR
1$\overline{CP1}$	4	13	2Q0
1Q$_1$	5	12	2$\overline{CP1}$
1Q$_2$	6	11	2Q$_1$
1Q$_3$	7	10	2Q$_2$
GND	8	9	2Q$_3$

Ordering Information

| PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD74HC390E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT390E	-55 to 125	16 Ld PDIP	E16.3
CD74HC390M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT390M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

2. Wafer for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

File Number **1838.2**
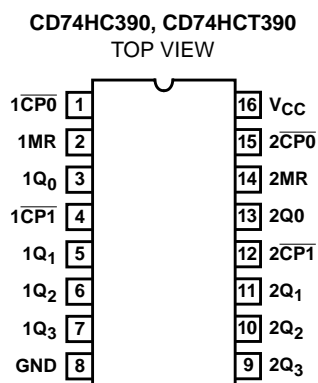
Functional Diagram
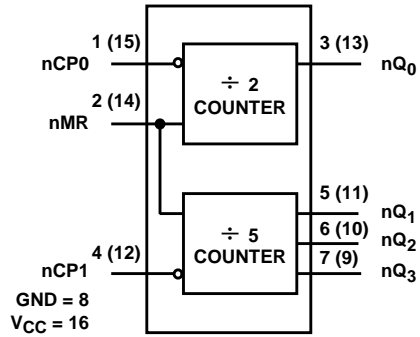
TRUTH TABLE

INPUTS		ACTION
CP	**MR**	
$\uparrow$	L	No Change
$\downarrow$	L	Count
X	H	All Qs Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care,
$\uparrow$ = Transition from Low to High Level, $\downarrow$ = Transition from High to Low.

BCD COUNT SEQUENCE FOR 1/2 THE 390

COUNT	OUTPUTS			
	Q0	**Q1**	**Q2**	**Q3**
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output nQ0 connected to n$\overline{CP1}$ with counter input on n$\overline{CP0}$.

B-QUINARY COUNT SEQUENCE FOR 1/2 THE 390

COUNT	OUTPUTS			
	Q0	**Q1**	**Q2**	**Q3**
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	H	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

NOTE: Output nQ3 connected to n$\overline{CP0}$ with counter input on n$\overline{CP1}$.

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Logic Diagram
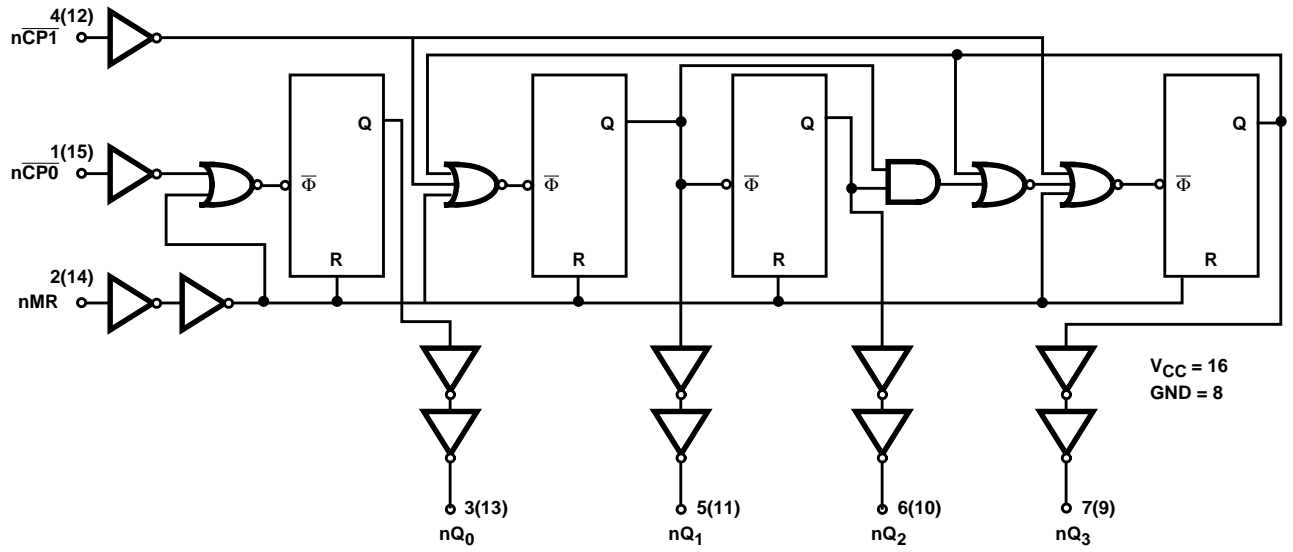
Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
    For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
    For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
    For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} $_{or}$ I_{GND} . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
    HC Types . . . . .2V to 6V
    HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
    2V . . . . 1000ns (Max)
    4.5V. . . . . 500ns (Max)
    6V . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (^{o}C/W)
    PDIP Package   90
    SOIC Package   190
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
    (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	I_O (mA)	V_{CC} (V)	25°C MIN	TYP	MAX	-40°C TO 85°C MIN	MAX	-55°C TO 125°C MIN	MAX	UNITS
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
$n\overline{CP0}$	0.45
$n\overline{CP1}$, MR	0.6

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Prerequisite for Switching Specifications

CHARACTERISTIC	SYMBOL	V_{CC} (V)	25°C MIN	TYP	MAX	-40°C TO 85°C MIN	MAX	-55°C TO 125°C MIN	MAX	UNITS
HC TYPES										
Maximum Clock Frequency	f_{MAX}	2	6	-	-	5	-	4	-	MHz
		4.5	30	-	-	24	-	20	-	MHz
		6	35	-	-	28	-	24	-	MHz
Clock Pulse Width, $n\overline{CP0}$, $n\overline{CP1}$	t_W	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Reset Removal Time	t_{REM}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns

Prerequisite for Switching Specifications (Continued)

CHARACTERISTIC	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Reset Pulse Width	t_W	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	11	-	13	-	ns
HCT TYPES										
Maximum Clock Frequency	f_{MAX}	4.5	27	-	-	22	-	18	-	MHz
Clock Pulse Width, $n\overline{CP0}$, $n\overline{CP1}$	t_W	4.5	19	-	-	24	-	29	-	ns
Reset Removal Time	t_{REM}	4.5	15	-	-	19	-	22	-	ns
Reset Pulse Width	t_W	4.5	13	-	-	16	-	20	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay (Figure 1) $n\overline{CP0}$ to nQ_0	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C_L =15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	30	-	37	-	45	ns
$n\overline{CP1}$ to nQ_1	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
			6	-	-	31	-	39	-	48	ns
$n\overline{CP1}$ to nQ_2	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	245	-	305	-	370	ns
			4.5	-	-	49	-	61	-	74	ns
			6	-	-	42	-	52	-	63	ns
$n\overline{CP1}$ to nQ_3	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
			5	-	15	-	-	-	-	-	ns
			6	-	-	31	-	38	-	46	ns
$n\overline{CP0}$ to $nQ3$ (nQ_0 connected to $n\overline{CP1}$)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	365	-	455	-	550	ns
			4.5	-	-	73	-	91	-	110	ns
			6	-	-	62	-	77	-	94	ns
MR to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	190	-	240	-	285	ns
			4.5	-	-	38	-	48	-	57	ns
		C_L =15pF	5	-	16	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	32	-	41	-	48	ns
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	C_L =15pF	5	-	28	-	-	-	-	-	pF

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

| PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES											
Propagation Delay (Figure 1)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
n$\overline{CP0}$ to nQ_0		C_L =15pF	5	-	17	-	-	-	-	-	ns
n$\overline{CP1}$ to nQ_1	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	43	-	51	-	65	ns
n$\overline{CP1}$ to nQ_2	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	55	-	69	-	83	ns
n$\overline{CP1}$ to nQ_3	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	42	-	53	-	63	ns
		C_L =15pF	5	-	18	-	-	-	-	-	ns
n$\overline{CP0}$ to nQ2 (nQ_0 connected to n$\overline{CP1}$)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	84	-	105	-	126	ns
MR to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	42	-	53	-	63	ns
		C_L =15pF	5	-	18	-	-	-	-	-	ns
Output Transition	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	C_L =15pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	C_L =15pF	5	-	32	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per multiplexer.

5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms
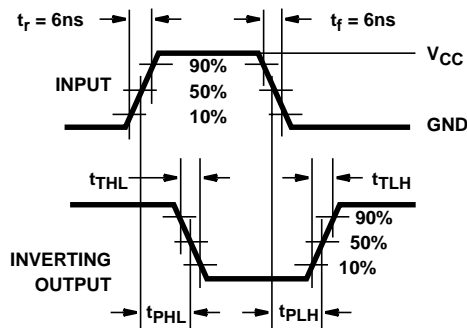
FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC
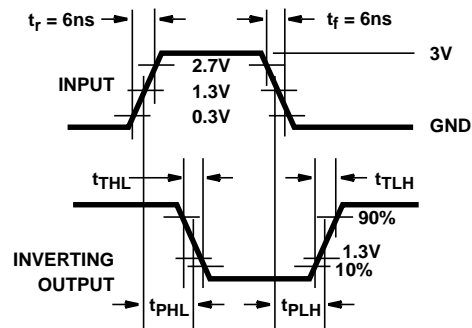
FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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